

IN THE CLAIMS

Please amend the claims to the following.

1. (Currently Amended) An apparatus comprising:
a trigger-response mechanism that includes at least one bank of user-programmable registers to identify a user-defined trigger event; and
a thread switch handler logic coupled to the trigger-response mechanism, ~~the thread switch handler~~ to perform a light-weight thread switch from a first thread to a second thread ~~invoke a second instruction stream responsive to an indication from the trigger-response mechanism that the user-defined trigger event has occurring~~ during execution of the first thread ~~a first instruction stream~~.
2. (Currently Amended) The apparatus of claim 1, wherein the user-defined trigger event includes a synchronous user-defined trigger event, ~~and wherein the thread switch handler is further to invoke the second instruction stream responsive to an indication from the trigger-response mechanism that the synchronous user-defined trigger event has occurred during execution of the first instruction stream.~~

1 3. (Currently Amended) The apparatus of claim 1, wherein the user-defined trigger
2 event includes an asynchronous user-defined trigger event, ~~and wherein the thread~~
3 ~~switch handler is further to invoke the second instruction stream responsive to an~~
4 ~~indication from the trigger-response mechanism that the asynchronous user-~~
5 ~~defined trigger event has occurred during execution of the first instruction stream.~~

1 4. (Currently Amended) The apparatus of claim 1, wherein the thread switch handler
2 logic to perform a light-weight thread switch from the first thread to the second
3 thread comprises: is to saving[[e]] a[[n]] first instruction pointer address for the
4 first thread ~~instruction stream~~ before setting a second instruction pointer address
5 for invoking the second ~~thread~~instruction stream.

1 5. (Currently Amended) The apparatus of claim 4, further comprising: a task queue
2 to receive the first instruction pointer address.

1 6. (Original) The apparatus of claim 5, wherein: the task queue further comprises a
2 memory location.

1 7. (Original) The apparatus of claim 5, wherein: the task queue further comprises a
2 register.

1 8. (Original) The apparatus of claim 1, further comprising: a plurality of event
2 counters coupled to the trigger-response mechanism, wherein each event counter
3 is to detect an atomic processor event.

1 9. (Currently Amended) The apparatus of claim 8, wherein the user-defined trigger
2 event includes an asynchronous trigger event based on one or more of the atomic
3 processor events, ~~and wherein the thread switch handler is further to invoke the~~
4 ~~second instruction stream responsive to an indication from the trigger-response~~
5 ~~mechanism that the asynchronous user-defined trigger event has occurred during~~
6 ~~execution of the first instruction stream.~~

1 10. (Currently Amended) The apparatus of claim 1, wherein the thread switch handler
2 logic is to perform the light-weight thread switch from the first thread to the
3 second thread transparently to an Operating System (OS) and without OS
4 intervention. ~~the thread switch handler is to save context information for the first~~
5 ~~instruction stream before invoking the second instruction stream.~~

1 11. (Currently Amended) The apparatus of claim 10, wherein: the thread switch
2 handler is further to save a light weight context for the first ~~thread instruction~~
3 ~~stream~~ in a memory location before performing the light-weight context switch
4 from the first thread to the second thread ~~invoking the second instruction stream.~~

1 12. (Currently Amended) The apparatus of claim 10, wherein: the thread switch
2 handler is further to save a light weight context for the first ~~thread instruction~~
3 ~~stream~~ in a register before performing the light-weight context switch from the
4 first thread to the second thread ~~invoking the second instruction stream~~.

1 13. (Currently Amended) The apparatus of claim 1, further comprising:
2 one or more user-programmable control registers coupled to the thread switch handler
3 logic;
4 the value of the one or more control registers to indicate a weight of the light-weight
5 ~~context information for the~~ thread switch from the first thread to the second thread. ~~first~~
6 ~~instruction stream to be saved responsive to invoking the second instruction stream~~.

1 14. (Currently Amended) A system comprising:
2 a memory to hold an instruction; and
3 a processor coupled to the memory, the processor including raw event detection logic
4 to detect at least one raw event, a user-addressable register to specify a user-defined trigger
5 event based on the at least one raw event, and a switch handler to invoke a helper thread
6 responsive to the occurrence of the user-defined trigger event.

1 15. (Previously Amended) The system of claim 14, wherein: the instruction includes
2 a marking instruction, when executed, to specify the user-defined trigger event in
3 the user-addressable register.

- 1 16. (Previously Amended) The system of claim 14, wherein: the instruction is a
2 trigger instruction; and raw event detection logic is to detect an opcode of the
3 trigger instruction when the trigger instruction reaches an execution phase of an
4 execution pipeline.
- 1 17. (Previously Amended) The system of claim 14, wherein: the processor further
2 includes a user-addressable control register to specify a weight of a context to be
3 saved responsive to invoking the helper thread.
- 1 18. (Currently Amended) The system of claim 14, wherein: the switch handler is
2 further to maintain minimal context information for a current thread before
3 invoking the helper thread, wherein the minimal context information includes a
4 context weight less than a full context weight by at least a weight of
5 excluding[[es]] traditional context information.
- 1 19. (Original) The system of claim 18, wherein: the excluded traditional context
2 information further comprises general register values.
- 1 20. (Original) The system of claim 18, wherein the minimal thread context
2 information comprises an instruction pointer address value.
- 1 21. (Currently Amended) A method comprising:

2 in response to detecting a user-specified trigger condition;
3 suspending execution of a first thread on a ~~[[single-]]~~threaded processor; and
4 utilizing hardware to switch save minimal context information of the first thread
5 with a second thread ~~for the current thread~~ without operating system
6 intervention, wherein the context information has a first weight that is
7 user-defined in a user-addressable control register.; ~~and~~
8 ~~invoking a second thread on the single threaded processor without operating system~~
9 ~~intervention.~~

1 22. (Original) The method of claim 21, wherein:

2 detecting a user-specified trigger condition further comprises determining that a trigger
3 instruction has been encountered.

1 23. (Original) The method of claim 21, wherein:

2 detecting a user-specified trigger condition further comprises determining that an
3 asynchronous condition specified in a marking instruction has been encountered.

1 24. (Currently Amended) The method of claim 21, wherein: the first weight includes
2 only an instruction pointer address. ~~utilizing hardware to save minimal context~~
3 ~~information further comprises saving an instruction pointer address value.~~

1 25. (Previously Amended) The method of claim 21, further comprising:

2 determining that the first thread should be resumed;
3 restoring the minimal context information for the first thread; and
4 resuming execution of the first thread without operating system intervention.

1 26. (Original) The method of claim 21, wherein detecting a user-specified trigger
2 condition further comprises:
3 receiving a marker instruction that specifies the trigger condition; and
4 monitoring a plurality of atomic event indicators to detect the trigger condition.

1 27. (Original) The method of claim 21, wherein detecting a user-specified trigger
2 condition further comprises: generating an asynchronous response to indicate that
3 the second thread should be invoked.

1 28. (Previously Added) A processor comprising:
2 event detection logic to detect a raw event;
3 user-programmable event logic coupled to the event detection logic to indicate a user-
4 defined trigger event, the user-defined trigger event to be based on at least the
5 raw event;
6 user-programmable context control logic to specify a weight of a context to be saved;
7 and
8 thread switch logic coupled to the user-programmable event logic and context control
9 logic, the thread switch logic, in response to the user-defined trigger event being
10 detected, to save a portion of a first context based on the weight of a context to
11 be saved that is to be specified in the user-programmable context control logic
12 and to spawn a helper thread without operating system intervention.

1 29. (Currently Amended) The processor system of claim 28, wherein the user-
2 programmable event logic includes at least a user-programmable event register,
3 and wherein the user-defined trigger event is to be programmed in the user-
4 programmable event register in response to execution of a user marking
5 instruction.

1 30. (Currently Amended) The processor system of claim 28, further comprising
2 trigger response logic coupled to the user-programmable event logic and the event
3 detection logic to detect the user-defined trigger event based on at least the raw
4 event, wherein the trigger response logic is to monitor for the user-defined trigger
5 event for a predetermined timeout period after execution of the user-marking
6 instruction.